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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,776	04/02/2004	Amitabh Jain	TI-34913A	2773
23494	7590	03/28/2006	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			BLUM, DAVID S	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/816,776

Applicant(s)

JAIN ET AL.

Examiner

David S. Blum

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/13/05.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

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This action is in response to the amendment filed 12/13/05.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 5, 7-9, 11-13, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mayur (US2003/0040130A1).

Mayur teaches all of the positive steps of claims 1-3, 5, 7-9, 11-13, and 15-18 except for explicitly teaching a temperature range of 1050-1350 degrees C..

Regarding claim 1, Mayur teaches providing a semiconductor (paragraph 0042), implanting a dopant species into the semiconductor (paragraph 0054) and annealing the implanted semiconductor at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, (Table II 1423 K (1150 C).

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As paragraph 0054 teaches a temperature above 1027 degrees C., and limits melting to only surface melting (occurs at 1150 C), it is obvious that Mayur has anticipated a temperature of at least 23 more degrees and therefore teaches 1050 degrees C.

Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface melting. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

These ranges are considered to involve routine optimization while it has been held to be within the level of ordinary skill in the art. As noted in *In re Aller* (105 USPQ233), the selection of reaction parameters such as temperature and concentration would have been obvious:

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art. Such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

One skilled in the requisite art at the time of the invention would have used any ranges or exact figures suitable to the method in the process of annealing regarding time and temperature using prior knowledge, experimentation, and observation with the

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apparatus used in order to optimize the process and produce the annealed structure desired to the parameters desired.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

Regarding claim 2, the implant is amorphizing (paragraph 0054).

Regarding claim 3, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 5, Mayur teaches providing a semiconductor (paragraph 0042), a patterned photoresist layer (paragraph 0051), implanting a dopant species into semiconductor (paragraph 0054), removing the photoresist (figure 2C shows patterned photoresist removed), and annealing with a solid phase epitaxy anneal (paragraph 0043, epitaxial, paragraph 0084, solid phase and paragraph 0047, conventional anneal). Although Mayur does not recite "solid phase epitaxy anneal, this is inferred from the process (same as the instant application) and that it is a solid phase anneal resulting in an epitaxial layer.) The anneal is at an ultra high temperature of 1050-1350

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degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

As paragraph 0054 teaches a temperature above 1027 degrees C., it is obvious that Mayur has anticipated a temperature of at least 24 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface temperature. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

These ranges are considered to involve routine optimization as recited above in regard to claim 1.

Regarding claim 7, the implant is amorphizing (paragraph 0054).

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Regarding claim 8, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 9, Mayur teaches providing a semiconductor substrate (paragraph 0042), a gate dielectric layer (insulator 208), a gate electrode (210) on the gate dielectric, implanting dopant species into the semiconductor adjacent the gate electrodes (paragraph 0053), annealing the implanted semiconductor with solid phase epitaxy anneal between 550 and 950 C (paragraph 0047, diffusing dopants between 800-1100 C), and annealing at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

As paragraph 0054 teaches a temperature above 1027 degrees C., it is obvious that Mayur has anticipated a temperature of at least 24 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface temperature. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less

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than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

These ranges are considered to involve routine optimization as recited above in regard to claim 1.

Regarding claim 11, the amorphizing implant is preformed prior to the dopant implant (paragraph 0054).

Regarding claim 12, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Regarding claim 13, Mayur teaches forming a MOSFET transistor (paragraph 0006), providing a semiconductor substrate (paragraph 0042), a gate dielectric layer (insulator 208), a gate electrode (210) on the gate dielectric, implanting dopant species into the semiconductor adjacent the gate electrodes (paragraph 0053), implanting with gate sidewalls (as shown in figure 2F), annealing the implanted semiconductor with solid phase epitaxy anneal between 550 and 950 C (paragraph 0047, diffusing dopants between 800-1100 C), and annealing at an ultra high temperature of 1050-1350 degrees C. (paragraph 0007, greater than 1300K (1027 C) and paragraph 0099, surface melting only allowed, thus temperatures around melting temperatures, table II 1423 K (1150 C).

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As paragraph 0054 teaches a temperature above 1027 degrees C., it is obvious that Mayur has anticipated a temperature of at least 24 more degrees and therefore teaches 1050 degrees C. Further, paragraph 0099 and Table II suggest that the temperature would not be above 1150 to avoid more than surface temperature. Thus Mayur is suggesting a range of about 1027-1150 degrees C., within the range of the instant claims.

Regarding the duration of the annealing, Mayur teaches the ultra high temperature anneal comprises times from 0.5 to 3 milliseconds (paragraph 0007 less than 50 milliseconds, paragraph 0009, recrystallization and dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

These ranges are considered to involve routine optimization as recited above in regard to claim 1.

Regarding claim 15, the amorphizing implant is preformed prior to the first dopant implant (paragraph 0054).

Regarding claims 16 and 17, the amorphizing implant (amorphous implant) is preformed prior to the second dopant implant (paragraph 0054, amorphizing implant performed prior to well implant and source/drain implant, two different species).

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Regarding claim 18, the amorphizing implant comprises arsenic or antimony (paragraph 0005).

Response to Arguments

3. Applicant's arguments filed 12/13/05 have been fully considered but they are not persuasive.

The applicant argues that Mayur does not teach the temperature range claimed.

However, Mayur teaches a temperature above 1027 degrees C, and suggests that temperatures above 1150 would have deleterious results (melting). Thus a range of 1027-1150 is suggested.

The applicant argues that Mayur relates to a specific type of annealing (pulsed laser) and not annealing in general. However, there are no limitations in the claims to preclude laser annealing.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "not pulsed laser annealing") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant further argues that Mayur does not teach the time duration of the anneal as claimed. However, Mayur teaches a time less than 50 milliseconds, and that reads

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on the claims. Further, Mayur dopant activation is complete in less than 100 nanoseconds (0.0001 milliseconds). Thus Mayur teaches a time range of 0.0001-50 milliseconds, encompassing the claimed range.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

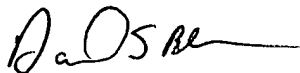
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David S. Blum

March 23, 2006